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A u.h.f. programmable digital field strength measuring receiver

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A UHF PROGRAMMABLE DIGITAL FIELD STRENGTH MEASURING RECEIVER

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Summary

A description is given of a field strength measuring receiver suitable for measuring broadcast television signals between 470 and 854 MHz. It represents a re-design of an earlier model with digital readout. It gives facilities for automatic operation which permits surveys to be carried out more effectively.

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1. Introduction

Over recent years u.h.f. field strength survey teams have used a receiver[1] which presented the measured field strength in digital display form relative to 1μV/m. Its readings include a preset correction factor for aerial gain, feeder loss, conversion from terminated voltage to e.m.f. and receiver sensitivity. The total correction is termed the 'K Factor' and its value is determined on a calibration range before commencing a survey.

For many reasons the K factor varies with frequency so that if a survey of several stations is simultaneously undertaken with a first generation digital receiver, K has to be changed for every channel. Furthermore, new requirements for more detailed survey work have rendered their manual tuners both unreliable, due to wear and tedious to use because, in most cases, many different channels have to be measured at each site.

As the principle on which the earlier receiver worked had proved satisfactory a second and more comprehensive design has been undertaken. By providing certain programmable options it is possible to meet the demand for simplicity of operation and readily measure the increasing number of stations on each survey tour.

A photograph of the receiver is shown in Fig. 1.

2. Specification of receiver

Frequency coverage: currently used channels in Bands IV and V (channels 21 to 68 inclusive) within the frequency range 470–854 MHz. Tuning is by channel number and any twelve channels can be set from any one of twelve push buttons by means of a memory system. The memory is retained for a minimum of one year with the set unpowered. An additional switch gives selection of sound or vision carrier on any channel and a continuous manual tuning control is provided for use if required.

Measuring range: 10μV to 1V e.m.f. from 50Ω source. The accuracy is better than ±1 dB over the whole range and field strength is displayed in 0·2 dB steps.

Input impedance: 50Ω.

Calibration: The receiver has an automatic internal calibration system and its output is corrected for any change in the receiver sensitivity which may occur after its field calibration.

External feeds: The receiver can provide a wide-band i.f. signal to a suitably modified television receiver so that the channel selected for measurement can also be viewed. An output is provided for a pen recorder, and can be adjusted to cover from 10 dB to 100 dB range per chart width, the range selected can be centred as required. The recorder output is 0 to 1 mA d.c. into 75Ω (specifically to suit Chessil Recorders used by BBC and IBA Research Departments). Auxiliary input/output sockets provide data in binary coded decimal of channel numbers for operating any external equipment. (e.g. standard field oscillator when calibrating, etc). The receiver provides power and control circuits for mast head preamplifiers and aerial polarisation changing equipment of the type used by BBC Research and Engineering Information Departments.

Frequency measurement: The receiver can display frequency offsets of vision or sound carrier frequencies up to ±199·9 kHz from the nominal channel frequency with an

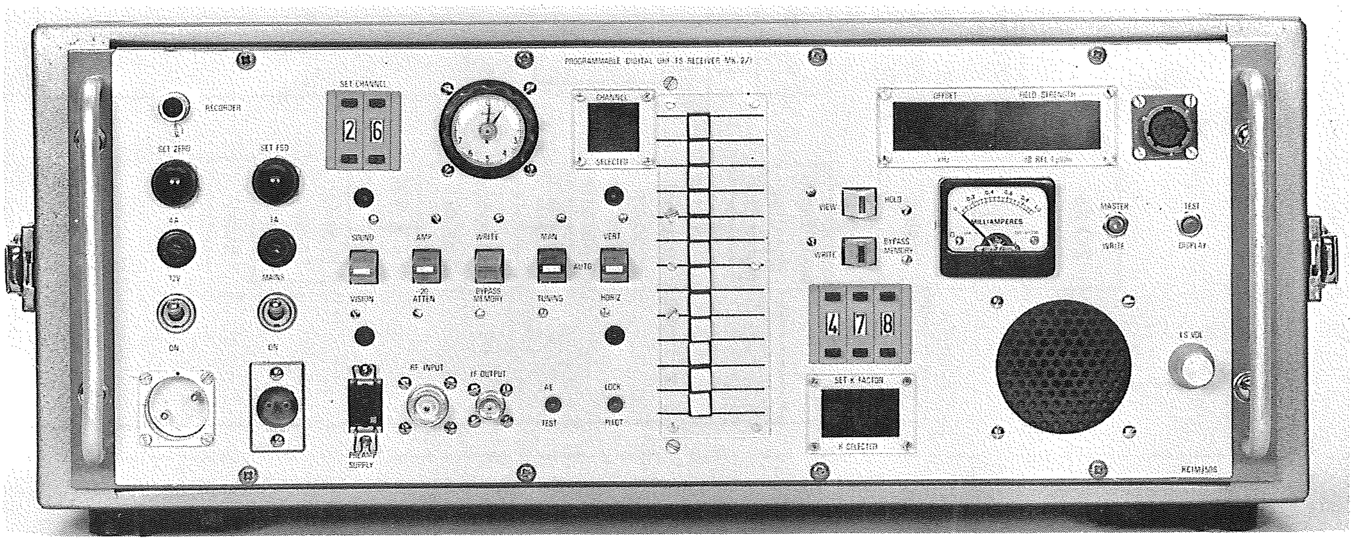

Fig. 1 - Photograph of receiver

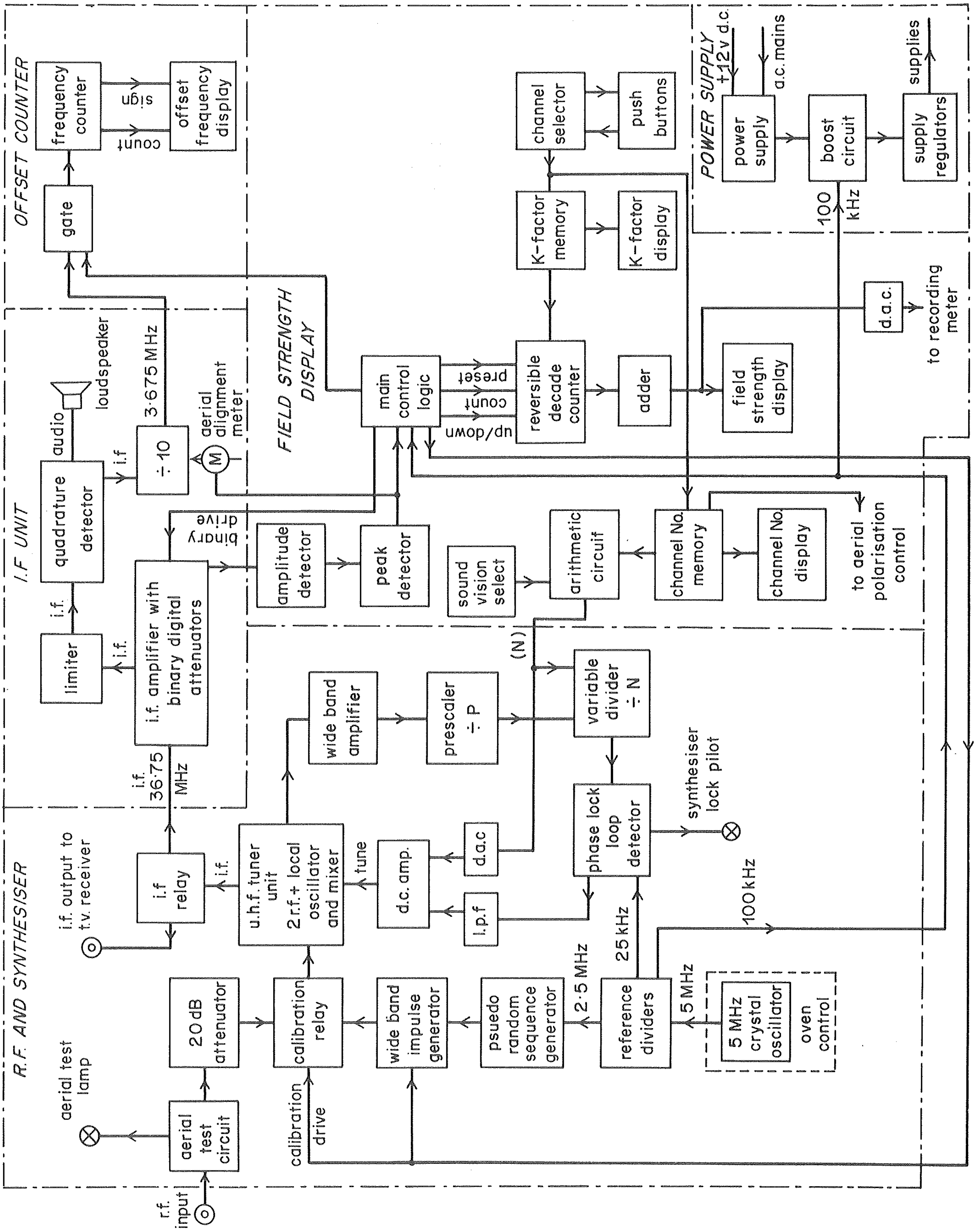

Fig. 2 - Block diagram of receiver

accuracy of ±100 Hz on all channels.

Tuning accuracy: The receiver employs a synthesised local oscillator and RF tuning system which sets the receiver to within ±100 Hz of the nominal channel frequency, the time to tune from one channel to another is less than 1 second. The channel tuning and offset display will fall within the specified frequency tolerance within 5 to 7 minutes from switch on.

Power supply: either a) 200–250V 50/60 Hz mains
or b) 12V (nominal) vehicle battery with negative earth.

The receiver consumption is 36 watts.

Case heater: Since the receiver specification calls for an operating temperature range of $0^{\circ}C$ to $50^{\circ}C$ a thermostatically controlled case heater is powered when the receiver is switched off. It is thereby possible to maintain an internal temperature in excess of $5^{\circ}C$ and avoid the circuit warm up period after the receiver has been left over night.

Dimensions: Standard MAJAR case 530 x 300 x 200 mm. Weight 10 kg.

3. Description

From the block diagram in Fig. 2 it can be seen that the receiver falls naturally into five sections.

1. The r.f. unit comprising the tuner, local oscillator synthesiser, calibration source and reference oscillator.
2. The intermediate frequency amplifier.
3. The field strength display system.
4. The offset frequency counter.
5. The power supplies.

3.1. The r.f. unit

The incoming signal is connected through an isolating capacitor to allow a small direct current to be circulated around the aerial and feeder system. In the first place this checks that there is, as normal, a short circuit to d.c. and operates an indicator lamp to confirm that the aerial connection is complete. Secondly it 'wets' the various plug and socket connections to reduce the likelihood of intermittent joints or rectifying contacts causing intermodulation in the presence of large signals. The signal is passed via a 20 dB overload attenuator to a standard commercial varactor tuner unit, comprising two r.f. amplifier stages and a local oscillator/mixer circuit. The first r.f. stage has an aperiodic input for optimum noise factor, and the interstage coupling in front of the second r.f. amplifier and the mixer are simple band pass circuits. The resultant signal is filtered to remove the r.f. and oscillator frequencies and connected to the i.f. system by a 'bottom C' coupling circuit. The coupling is chosen to include the cable capacity of the coaxial link to the television receiver. A small amount of local-oscillator energy is extracted from the tuner by a capacity probe to provide the input signal for the synthesiser. The extracted signal is amplified by a thick-film wide-band amplifier to a level sufficient to operate the high-speed pre-scaler which divides by factor P the local oscillator frequency (508 MHz to 884 MHz) giving a suitable value for the programmable counter which controls further division by factor N.

As the receiver has to tune to either sound or vision, the local oscillator has to shift in steps of 6 MHz or 8 MHz and so it is convenient to produce a 2 MHz frequency change with one increment of N. Therefore, if the oscillator incremental frequency is 2 MHz and P = 80, the synthesiser reference frequency must be an eightieth of 2 MHz, viz. 25 kHz. Also the values required for N vary from 254 to 442. However, it is convenient to split division by P into two stages of ÷ 40 before ÷ N, and ÷ 2 afterwards, and to operate the counter over a range of input frequencies 12·7 to 22·1 MHz. A readily available 9-bit binary counter can be used which has a maximum ratio of 512. It commences countdown from a pre-loaded ratio and when the zero state of the counter is detected it is again pre-loaded with every cycle giving a single output pulse to the next circuit.

The channel number required is set into the receiver from a two-decade switch and, since the highest channel number is 68, only seven wires are required, four for the units and three for the tens using binary coded decimal (BCD). The information is stored in the memory circuits and, with BCD rather than nine-bit binary, the memories used need only have a capacity of four 8-bit words. A spare bit then becomes available and is used for other purposes described later, but it is now necessary to convert the BCD code to binary; this conversion is performed in the arithmetic circuit.

It can be shown that a convenient conversion from channel number to the required value of N is given, for vision channels, by

$$N_v = 4(C-16) + 234$$

where C is the channel number. For sound channels it is given by

$$N_s = 4(C-16) + 237$$

The increase of 3 from 234 to 237 raises the local oscillator frequency by 3 x 2 MHz. The conversion is performed in four 4-bit binary adders, which form the arithmetic circuit.

The synthesiser control loop is completed by the phase/frequency comparator which delivers a d.c. output via amplifiers to the varactor diodes in the tuner. The range of voltage required to cover channels 21 to 68 is from 0·3V to 28 volts so the amplifiers are powered from supply rails of −5 and +33 volts. If required provision is made to open the control loop by means of a switch on the front panel and substitute a 10 turn "helipot" as a manual tuning control. The switch also provides a blanking signal for the channel number display.

The d.c. amplifier chain includes feedback circuits arranged to form a low pass filter and so removes any reference-frequency component from the varactor control volts thereby avoiding unwanted local oscillator frequency modulation.

The reference-frequency supply at 25 kHz is derived by a chain of dividers, from a 5 MHz oven stabilised crystal oscillator which has a frequency stability of 1 part in 10^8 and a warm up time of about five minutes. The same divider provides various other frequencies for use elsewhere in the receiver.

The time taken for the synthesiser to settle at a new frequency depends on the division ratio of the programmable counter, and the phase locked loop time constant. A more rapid settling time is achieved by using a simple network to convert the ÷ N counter input from a digital to an analogue signal. The resultant analogue voltage is then added to the output of the comparator so that any change of frequency produces amplified error information and the comparator rapidly adjusts frequency to phase lock the local oscillator to the reference source. Only the most significant bits of the ÷ N binary signal is used in this system since the reduction of settling time is required only for large changes of frequency.

When the comparator reaches phase lock at the two inputs, the in phase condition is detected by an auxiliary circuit to operate the 'lock' pilot and show that the receiver is correctly tuned.

The calibration source for the receiver is an impulse generator using a pair of step-recovery diodes. These diodes behave in a conventional way when forward biased but when they are suddenly reversed they continue to conduct for a short time before switching off abruptly, thereby generating a very steep waveform. In the circuit used the first diode is cut off by applying a pulse from a differentiating circuit. The pulse it produces then operates a second diode to generate a short pulse with a very rapid rise time across a 50 ohm resistor to become the source for the calibrator. The spectrum of the pulse is substantially flat to 1 GHz. Thus a line spectrum is produced, with the line spacing dependent on the frequency at which pulses are applied to the step recovery diodes. The pulse repetition frequency comes from a pseudo-random sequence generator comprising a shift register and a bi-stable flip-flop clocked by a 2·5 MHz output from the reference crystal oscillator. This system simulates a "white-noise" source but delivering more power than conventional semiconductor white-noise sources.

3.2. The i.f. unit

The 36·75 MHz tuner output is fed to the i.f. amplifier via a relay, which can be operated to divert the i.f. to a television receiver. When the relay switches the tuner output to the digital i.f. amplifier, the wide-band video circuit is removed and the measuring receiver bandwidth is determined by a narrow filter in the i.f. unit.

Following a tuner isolating amplifier there are four dual cascode stages which perform the digital switching of the attenuators. Detailed description of the operation of these stages has been given elsewhere.[1] The last i.f. amplifier feeds the amplitude detector and a pre-limiter stage. Although the amplitude detector receives only a narrow band signal (±300 kHz) it is able to produce a sync pulse waveform which is sufficiently accurate for measurement purposes by passing the waveform to a detector with a rapid rise characteristic and a long decay time constant. After peak rectification the resultant d.c. is applied to a level gate which generates a sharp edge when the voltage rises above a fixed reference value. The edge is then used to stop the binary counter which operates the i.f. attenuators. In order to speed up the operation of the receiver the first steps of attenuation are switched out at the rate of 1000 steps/sec until the output of the peak detector reaches about 1 dB below the threshold level of the stop signal. The rate is then reduced to 100 steps/sec so that the detector has time to reach a true peak value as each step of attenuation is removed, thereby preventing overshoot. This rate reduction is achieved by an additional level detector which operates just before the main detector produces the stop signal. To ensure that the peak detector integrating circuit always starts from the same voltage a clamp transistor discharges the associated capacitor when the binary counter is reset and all the attenuation is reinserted.

A second output from the last i.f. stage is connected via a pre-limiter stage to the main amplitude limiter and quadrature detector. This circuit either demodulates the sound carrier or if tuned to the vision channel provides an i.f. output stripped of modulation to drive the frequency counter which detects the frequency offset.

Due to the narrow i.f. bandwidth, the digital receiver cannot tune to both sound and vision carriers simultaneously. However, when tuned to vision and used in conjunction with an intercarrier television receiver, it is possible to detect both together. By arranging that the sound volume of the television receiver is controlled by a d.c. passed over the i.f. coupling cable between the receivers, the sound level adjustment is conveniently transferred to the front panel of the digital receiver. Furthermore, when the television set is connected, the digital receiver sound output is muted.*

3.3. The field strength display system

The whole receiver is controlled by the main logic circuit which generates all the required timing waveforms and governs events in each section of the receiver. The sequence of operation is based on a shift register which is clocked by a 1 kHz obtained from the 5 MHz reference. The cycle commences when a signal is applied to the data input of the shift register. As this signal moves along the register, the first function causes the i.f. attenuator binary counter to reset to maximum attenuation. At the same time the reversible decade counter is preset to the number of decibels as stored in the K factor memory for the particular push button on the channel selector in use. Next the decade counter is set to count in an upwards direction and the calibrator pulse generator triggered. After a short delay for various relays to operate, clock pulses at 1 KHz are applied to both binary and decade counters. Each pulse causes the binary counter to remove a 0·2 dB step of attenuation in the i.f. amplifier, whilst the decade counter increases its count from the programmed K value. When the calibration signal at the i.f. output reaches the reference level of the rate detector the 1 KHz clocks are replaced by 100 Hz clocks and counting continues at the slower rate. When counting is complete the stop gate is operated causing the main logic shift register to re-set the i.f. binary counter and inhibit the calibrator. Next, the r.f. signal to the receiver replaces the calibration signal and the decade counter is reversed so that it counts in a downwards direction. At this point the decade counter contains a value equal to K + C where C is the number of decibels of attenuation removed to equate the calibration signal to the detector reference level. Clocking of the two counters now recommences, but this time, the incoming signal is measured, so that when the detector reference level is again reached the decade counter contains K + C − M where M is the incoming signal level. This total value is now transferred to latches by a pulse from the shift register and the output of the latches recorded in decibels above 1μV/m on the field strength display which uses light-emitting diodes. The shift register then resets and the whole cycle recommences. Latches sustain the display until the following cycle is over and an updated read out is presented. Suppose now that for some reason the receiver r.f. gain is increased by S dB. The value of K remains unchanged but C will be reduced by the amount S so that at the end of the calibration cycle the decade counter will contain K + (C − S). It follows that on the measure cycle M will also be reduced by S. Therefore the final condition will be K + (C − S) − (M − S) = K + C − M as before. In the case of the i.f. amplifier, a gain change will not be cancelled but instead, cause a departure from the pre-determined logarithmic transfer response. However, it is known from previous receiver designs which use the same i.f. circuit, that if such changes do occur they are rare and normally very small. Thus the digital receiver is self compensating in terms of any significant gain changes.

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* The design features of this arrangement for feeding a domestic receiver are due to D.M. Hodge who has also contributed substantially the whole project.

If the incoming signal is so low that all the i.f. attenuation is removed, the maximum-gain condition is detected and initiation of the count cycle withheld. At the same time the display is blanked except for the last figure which shows an L as an indication that the signal is either absent or too low to measure. Conversely, if the incoming signal is so large that all the i.f. attenuation is inserted, the minimum-gain condition is detected and a second set of limit gates operate to display an H showing that the signal is too high. The operator can escape the overload condition by manually introducing a further 20 dB attenuator in the receiver input circuit, with a key on the front panel. This will normally bring the signal back into range and re-start the measurement cycle. To avoid any measurement confusion the value of the manual attenuator is automatically added to the displayed figure. The use of a high-precision attenuator for this purpose is unnecessary as the actual value of the attenuation, to the nearest 0·1 dB, can be preset on the adder circuit card, thereby removing the need for an expensive component. So long as the attenuation is about 20 dB and flat over the range 470 MHz − 890 MHz, adjustment of the preset switches can be made in the laboratory when the receiver is commissioned.

During a frequency change and while the synthesiser is settling, the field strength display is incorrect. Therefore the main logic is arranged to blank the display until the phase detector has locked. If the receiver is set to manual tune the phase loop is permanently open and so it is necessary to inhibit the blanking signal otherwise the display would fail to read.

To prevent the calibration system interfering with either picture display or the vision frequency offset counter further restrictions are placed on the cycling procedure when both the 'view' or 'offset' modes are selected. However, the main logic does undertake a single run through the i.f. attenuation settings to ensure sufficient signal is available at the limiter to give a correct offset count.

3.4. The frequency-offset counter systems

The offset measuring system counts the intermediate frequency and displays the error between the actual value and the nominal 36·75 MHz. Offsets are only displayed to ±100 Hz and up to ±199·9 kHz and so a 4 digit display is all that is necessary with just the least significant digits of the counter presented. Any higher offset is unlikely to be encountered and blanks the display by substituting a row of dots to indicate that the error is outside the range of measurement. The input to the counter is from the i.f. amplifier through a divide by twenty circuit so that the counter proper is operated at 1·8375 MHz. Hence the gate time required by the counter is 0·2 seconds and the counter operates every 0·4 seconds. The 10 Hz control square wave is derived from the local oscillator synthesiser circuit. (See Fig. 3). An equivalent value equal to the nominal i.f. is pre-loaded into the counter which then counts down towards zero. If the offset is positive then the i.f. will be low and the counter will not have time to reach zero. The residual count is then the difference between real and nominal carrier frequency and is displayed together with a + sign. When the offset is negative, the i.f. is high and the counter passes through the zero to continue a count from 0000 to 9999 to 9998 etc. Under these conditions the counter output is passed via a nines complement circuit to cause the display to read from 0 to 0001, 0002, etc. and at the same time the sign is changed from + to −. When checking a sound offset the frequency modulation does not noticeably affect the counter reading because the deviation averages out over the 0·05 second gate period.

3.5. Power supplies

The digital receiver is primarily designed for use in service planning vans and so a 12-volt negative earth battery will be the normal source of power. In practice vehicle supplies vary from 10 to 17 volts so it is unsafe to design for a constant input. A series safety rectifier, is fitted to protect the receiver from the application of reversed polarity this also reduces the actual voltage available to 9·6 and 16·6. Some form of boost system is therefore

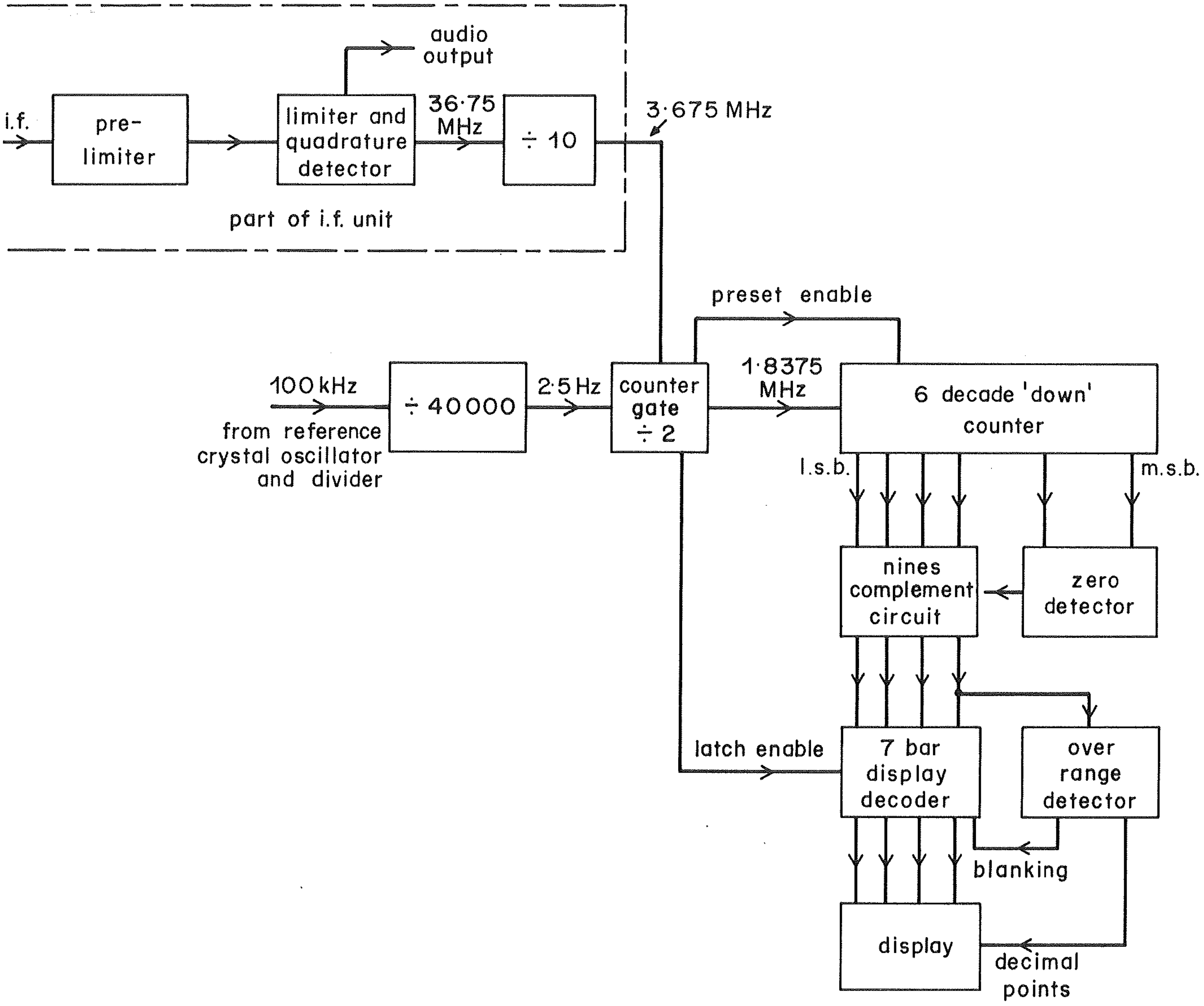

Fig. 3 - Block diagram of offset counter

required and in previous receiver designs an ultrasonic oscillator, followed by high speed rectifiers has been the method. Experience has shown that this arrangement is subject to fairly frequent breakdowns because, if for any reason the oscillator fails to start, the associated transistor will almost certainly burn out due to excessive current flow. Also the circuit can give rise to voltage spikes and high frequency disturbances on the supply rails, both of which are extremely difficult to suppress.

Therefore, in the receiver the incoming supply is first stabilised at 8 volts by a conventional series regulator and then boosted to 18 and 30 volts by externally excited transistor switches. The main components in the boost circuit are a ferrite transformer followed by high speed rectifiers which have a switching time of about 1μs. The transformer is energised by two push-pull transistors driven at 50 kHz, from a waveform available in the synthesiser reference crystal dividers. As the crystal circuit is powered from the 8 volt regulator, the booster is self starting. Should the drive fail the transistors are instantly cut-off and protected by a NOR gate on each input which closes as soon as the drive waveform ceases. Although this system uses more components than a conventional high frequency supply, it is extremely efficient with about 92% of the input power available at the boosted voltage. Consequently, heat dissipation is no problem. The application of bi-phase rectification to an almost perfect square wave and the use of bifilar windings on the transformer, ensures that the d.c. output is virtually free of ripple. The reservoir capacitors then become a reasonable size to give adequate smoothing at the required currents. Further card mounted regulators then produce 12 and 24 volt rails. A second unit using the same general principle is included on the synthesiser card to provide a regulated 33 and −10 volts for varactor diode tuning. The 50 Hz mains supply consists of a 12 volt, 4 amp, power pack which is substituted for a vehicle battery.

Finally, there are two auxiliary power requirements to describe, one of 4·5 volts and another of 12 volts. The 4·5 volt supply comes from small re-chargeable nickel cadmium cells to maintain the information stored in the two memories when the receiver is switched off. The current consumption is very small, less than 1μA, and even allowing for a certain amount of leakage the memories can be expected to retain data for at least a year. Every time the receiver is powered a charging current flows to the nickel cadmium battery.

To control the plane of polarisation of the measuring aerial, either vertical or horizontal, a 12 volt solenoid-valve is attached to the rear of the aerial and rotates the elements through 90°. Mention was made in section 3.1. about spare storage capacity in the channel number memory and if required, this can be programmed to store the appropriate polarisation for each transmitter entered in the channel register. On the front panel there is a manual polarisation control switch to override the memory at any time and also a socket into which may be plugged the mast-head solenoid cable.

4. Construction and maintenance

Clearly the programmable digital receiver is a complex scientific instrument, so ease of construction and maintenance must be a prime requirement if it is to give good service. To this end, the component layout is based on a number of small plug in assemblies fitted to a mother board. By employing a large number of exchangeable cards, each containing a small part of the circuit, it is possible to adopt either a 'throw-away' approach to maintenance or if time permits investigate the faulty assembly after the receiver has been returned for service. There are also four redundant bits per word in the K factor memory brought out to spare tags on the printed circuit cards and they may be used to replace a defective memory cell rather than renew the whole memory chip. Moreover, any improvements to circuitry or components which, are found to be desirable as technology progresses, can easily be incorporated. For example, by changing the plug in u.h.f. commercial tuner for a readily available v.h.f. counterpart and replacing a single card in the synthesiser, the receiver can measure television System–I signals in Bands I and III. This should be a valuable facility which will extend the useful life of the design when work is undertaken in connection with re-engineering the v.h.f. television bands.

5. Conclusions

The receiver described is a considerable advance over its predecessor both in measurement range and stability as well as providing many extra facilities. Its applications could extend beyond field strength surveying, including use as a diagnostic tool when dealing with complaints from the public, a long term recording receiver for the assessment of re-broadcast links or for offset checking at transmitter monitoring centres.

6. References

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